Minimum Energy Sub-Threshold CMOS Operation Given Yield Constraints

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**ABSTRACT**

Digital circuits operating in the sub-threshold region are significantly slower than above-threshold circuits, but they provide very-low-power operation. A major issue with sub-threshold circuits is the impact that fabrication process variations have on them; at sub-threshold voltages, deviations in individual transistors' threshold voltages have substantial effects which can cause circuits to fail. This project addresses whether a designer should, given a constraint on functional chip yield, increase supply voltage or increase transistor size to meet this constraint while maintaining the smallest energy consumption possible. Conclusions have yet to be reached, as simulations are not complete due to time constraint and, thus, final analysis has not been completed. Further work will continue early 2013.

**1. INTRODUCTION**

As industrial fabrication technologies become capable of creating increasingly smaller devices, the number of transistors on modern chips has dramatically increased. Moore’s law predicts an exponential growth of the number of transistors in integrated circuits in the future and has held true in the industry for over 50 years. Without technological breakthroughs, this also implies an exponential growth of power density for modern chips; clearly, this model cannot continue forever. In fact, the industry has already hit limitations due to excessive power density.

One possible solution to this problem is to lower the power supply voltage (Vdd) of circuits. As shown in the power dissipation equation, power is quadratically dependent on Vdd level:

(1)

Thus, by reducing Vdd, we effectively decrease energy. Of course, reductions in Vdd also reduce performance by reducing circuits’ operating currents. Sub-threshold circuits run at Vdd levels below the threshold voltage level of transistors and are a promising new method to dramatically reduce energy consumption in chips.

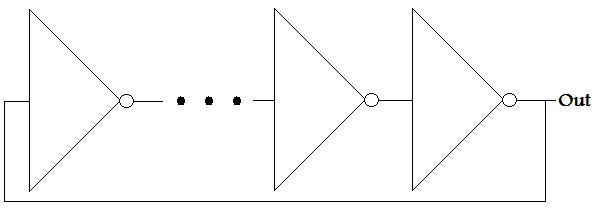
Lowering Vdd to sub-threshold levels increases the risk of logical circuits failing, which decreases overall yield. This is due to fabrication variations in transistor threshold voltages (Vth), which sub-threshold operating current values are extremely sensitive to. In order to counteract this, transistors can be resized. We started with the assumption that the failure rate of a given technology increases exponentially as Vdd is lowered and decreases quadratically as transistor sizing is increased. Finally, given these assumptions, it was our goal to derive an optimum sizing and Vdd level to minimize energy consumption while maintaining a reasonable yield.

Section 2 is an overview of ring oscillators and how we use them to test our assumptions. In Section 3, we discuss the changes we needed to make to enable efficient Monte Carlo analyses. Section 4 is a discussion on our simulation results. Section 5 is a conclusion to the paper.

**2. Background**

**2.1 Ring Oscillator**

In order to test our assumptions about the effects of sizing and Vth on energy consumption, we needed a simple circuit that could be simulated for thousands of tests in a reasonable amount of time. We decided to run simulations on a ring oscillator. Ring oscillators are composed of an odd number of cascaded inverters, with the final inverter output connecting to the initial inverter input (Fig. 1). Due to the odd number of inverters, the output value must be the inversion of the starting input value. Since this final value feeds back into the cascaded inverter chain, the result is an oscillating signal that takes a measureable time to propagate through the ring oscillator. By increasing the number of inverters in the cascaded chain, the period of oscillation increases.

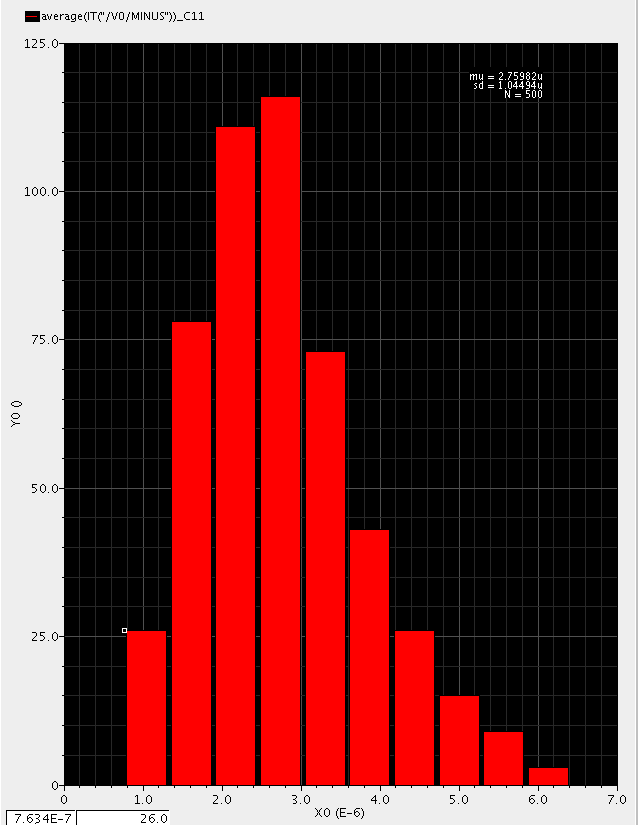


**Figure 1. Ring oscillator schematic.**

In order to use the ring oscillator to calculate failure rate, we set the initial voltage value to 0 in order to begin the oscillation. The signal that propagates through the ring oscillator has a measurable frequency that is affected by the Vdd level, transistor sizing, and number of inverters composing the ring oscillator. Thus, by measuring the frequency (or lack thereof) we can easily determine a failure for an inverter where variations could create a strong PMOS and a weak NMOS or vice versa. The variations in this case would cause the inverter to evaluate to an incorrect value and thus cause the rest of the inverter chain to either latch to a high or low value. Thus, by measuring the frequency of the ring oscillator output using Cadence Virtuoso, we were able to automatically measure the failure and yield rates.

**2.2 Monte Carlo Simulations**

We ran Monte Carlo simulations in order to randomly vary threshold voltage values based on a Gaussian distribution with an assigned standard deviation. By running many Monte Carlo simulations, we were able to obtain statistical results for realistic transistors with PVT variations. Mainly, we looked at the frequency of the ring oscillator to ensure that it was functioning correctly. Variations due to the Monte Carlo analysis assign each transistor a threshold voltage deviating from its original value based on the percent deviation we assigned. This causes ring oscillator frequencies to either be higher or lower than the expected value because variations may either improve or degrade the frequency (figure 2).



**Figure 2. Frequency Variation Histogram**

In our ring oscillator schematic, we concluded that a 101 inverter chain was optimal to perform simulations in a reasonable amount of time. In addition, we also decided to run 100 Monte Carlo simulations at each corner. Knowing that we needed to run thousands of Monte Carlo simulations to obtain meaningful results, it was important for us to develop methods such as evaluating frequency for a given simulation to determine failures due to varying Vth values in an efficient manner.

**3. SIMULATION SETUP**

In order to run Monte Carlo simulations varying Vth, we needed model files that allowed simulation of individual transistor fabrication process variations. We edited FreePDK NMOS and PMOS transistor model files to include instance specific Vth values that could be modified using a Gaussian distribution of Vth values.

Because our model files were non-commercial and more simplistic compared to industry standard model files, there was no Vth dependency on transistor sizing. In real silicon transistors, Vth has a first order dependency on transistor sizing [1]:

(2)

In order to force this effect in our model files, we hardcoded a simple dependency. In the future, when we use more accurate model files, this dependency will be better defined.

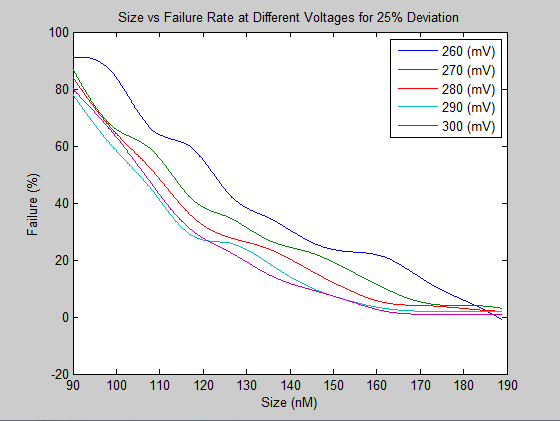
Due to simulation software limitations, we could not simulate ring oscillators with thousands of cascaded inverters nor produce massive amounts of Monte Carlo trials. In order to overcome this constraint, we ran short initial simulations to discover the corners where failures first started to occur. Because of the fact that we could not simulate 1001 inverters at a 10 percent standard deviation, we had to increase the standard deviation in order to produce failures with 101 inverters. We found that with a 25 percent deviation, the best case scenario of 300 mV and double the minimum sizing would result in at least one measured failure in 100 trials. By increasing the deviation for threshold voltage to 25 percent, failures were guaranteed for all the other cases since they were worse than the best case. Simulations were conducted at voltages of 260 mV, 270 mV, 280 mV, 290 mV, and 300 mV while sweeping sizes from 90 nm to 180 nm in 10% increments. In addition, we recorded the current at each corner for further energy analysis.

**4. SIMULATION RESULTS**

**4.1 Size and Voltage versus Failure**

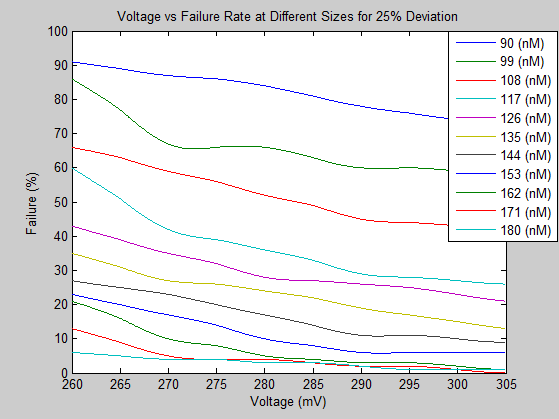
With our simulation data, we interpolated the values in Matlab and plotted a family of voltage curves for size vs. failure rate. The same process was also completed to obtain a voltage vs. failure rate graph.

Our first two simulations were conducted in order to verify the trend that we had predicted earlier. For the case of size versus failures, we saw the predicted trend where failure rate decreased exponentially when sizing was increased from 90 nanometers to 180 nanometers (Fig. 3).



**Figure 3. Size vs. Failure**

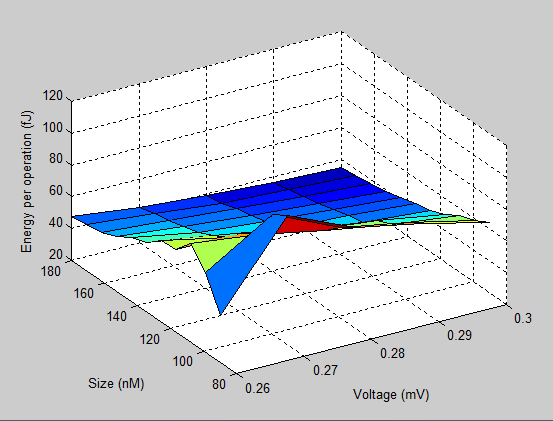
The next simulation result we obtained was voltage versus failure rate (Fig. 4). In comparison to figure 3, size seems to affect the failure rate more than voltage as seen by the more flat curve in figure 4. We determined that this was caused by our Vth sampling, which was biased towards the middle of a Gaussian distribution.



**Figure 4. Voltage vs. Failure**

**4.2 Determining the Optimal Point**

From these curves, we could choose a specific failure rate, and a corresponding voltage, size, and current could be obtained. By using a 3-D plot, we plotted voltage vs. size on the x and y axes while plotting energy per operation on the z axis (Fig. 5). We still need to take more measurements to obtain a plot that will allow us to define a true minimum energy point.



**Figure 5. Energy vs. size and voltage**

**5. CONCLUSION**

After further data is collected, we will be able to reach a conclusion on the minimum sizing and Vdd level needed to obtain minimum energy consumption given a yield requirement.

**6. Further Research**

We plan on working with a commercial model library, which will have more realistic Vth values that depend on other transistor parameters. We also plan on obtaining our own copy of Cadence and using it to run simulations. Because most of our simulations were done on university-owned Linux servers, simulations were very slow and large inverter chains, such as a 1001 cascaded inverter chain we attempted, would cause Cadence to crash. By being able to simulate with a larger inverter chain with more Monte Carlo simulations at each corner, we could produce more accurate data and smoother graphs.

**7. ACKNOWLEDGEMENT**

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**8. REFERENCES**

[1] Ye, Y., Liu, F., Nassif, S., Cao, Y. *Statistical Modeling and Simulation of Threshold Variation under Dopant Fluctuations and Line-Edge Roughness*. Design Automation Conference, 2008.